

AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1 1. (Currently Amended) An apparatus for performing the addition of a
2 propagate, kill, and generate recoded numbers, said apparatus comprising:
3 a circuitry configured to receive at least a first operand and a second operand,
4 the first and second operands comprising respective first and second propagate, kill,
5 and generate recoded number representations of respective first and second binary
6 operands;
7 a first carry-save adder configured to add said first operand and said second
8 operand to generate a third propagate, kill, and generate recoded number
9 representation; and
10 a modified carry-save adder configured to receive the third propagate, kill, and
11 generate recoded number representation from the first carry-save adder, add the
12 separate propagate, kill, and generate bits of the third propagate, kill, and generate
13 recoded number representation in accordance with a carry-in bit to, and generate a
14 sum value and a carry value.

1 2. (Original) The apparatus of claim 1, wherein said sum value and said
2 carry value are dual rail encoded values.

1 3. (Canceled)

1 4. (Previously Presented) The apparatus of claim 1, wherein said circuitry
2 is configured to receive and apply a carry-in value to the modified carry-save adder.

1 5. - 6. (Canceled)

1 7. (Currently Amended) A method for processing propagate, kill, and generate
2 representations of respective first and second binary operands, comprising:
3 receiving a carry-in value and a first and a second propagate, kill, and generate
4 representation of respective first and second binary operands;
5 adding the first and second propagate, kill, and generate representations to generate
6 a third propagate, kill, and generate representation; and
7 mathematically combining the third propagate, kill, and generate representation ~~and~~
8 in accordance with the carry-in value to generate a sum value and a carry value.

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1 8. (Previously Presented) The method of claim 7, wherein said step of
2 mathematically combining comprises adding the third propagate, kill, and generate
3 representation and the carry-in value.

1 9. (Canceled)

1 10. (Previously Presented) The method of claim 7, wherein said step of
2 mathematically combining further comprises generating dual rail encoded values.

1 11. (Previously Presented) The method of claim 7, further comprising:
2 generating a carry-out value responsive to the adding.

1 12. - 22. (Canceled)
